Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims

1. (Original) A system of integrated circuit components defining a plurality of nodes and a random access memory (RAM) connected to each node, each node comprising:

at least one functional unit configured to carry out a predetermined processing function;

a communication mechanism configured to manage and control communication of information with other nodes;

a memory controller configured to control writes to and reads from the RAM connected to the node;

wherein the system is further configured to permit read access to a RAM by a plurality of the nodes in the system, but is further configured to limit write access to a RAM to only the node to which the RAM is connected.

2. (Original) The system of claim 1, wherein the system is a computer graphics system.

3. (Original) The system of claim 1, wherein the at least one functional unit is one selected from the group consisting of a texture mapping component, a geometry accelerator, a shader, a z/blend component, a rasterizer, a tiler, and a cache controller.

4. (Original) The system of claim 1, wherein each node further includes control means for controlling the use and access of memory storage by remote functional units.

5. (Original) The system of claim 4, wherein the control means includes a memory segment containing at least one work queue, the work queue being in the form of a first-in-first-out instruction queue for the at least one functional unit.

6. (Original) The system of claim 5, wherein the work queue contains a plurality of messages.

7. (Original) The system of claim 6, wherein messages may be communicated between different nodes under control of the control means.

8. (Original) The system of claim 1, wherein the plurality of nodes are interconnected via a plurality of serial communication links.

9. (Original) The system of claim 4, wherein the RAM is segmented to include at least one segment dedicated to the control means of the connected node and at least one additional segment dedicated to carrying out a functional operation of the system.

10. (Canceled).

11. (Original) A system of integrated circuit components comprising:

a plurality of nodes interconnected by communication links;

a random access memory (RAM) connected to each node;

at least one functional unit integrated into each node, each functional unit configured to carry out a predetermined processing function;

each node containing a coherency mechanism configured to permit only read access to the RAM by other nodes, the coherency mechanism further configured to permit write access to the RAM only by functional units that are local to the node.

12. (Original) The system of claim 11, wherein a work queue comprises at least one message, the at least one message containing an instruction of the at least one functional unit of the associated node.

13. (Original) The system of claim 12, wherein messages may be communicated between different nodes under control of the control means.

14. (Original) The system of claim 13, wherein the plurality of nodes are interconnected via a plurality of serial communication links.

15. (Currently Amended) A system of integrated circuit components comprising:

a plurality of nodes interconnected by communication links;

a random access memory (RAM) connected to each node, wherein the plurality of RAMs in the system are configured as a unified RAM;

at least one functional unit integrated into each node, each functional unit configured to carry out a predetermined processing function; and

a coherency mechanism within each node, the coherency mechanism configured to permit ~~only~~ read access to a given RAM by any of the plurality of nodes, the coherency mechanism further configured to permit write access to the given RAM only by functional units of the node connected to the given RAM.

16. (Previously presented) The system of claim 15, wherein the at least one functional unit is one selected from the group consisting of a texture mapping component, a geometry accelerator, a shader, a z/blend component, a rasterizer, a tiler, and a cache controller.

17. (Previously presented) The system of claim 15, wherein the coherency mechanism includes a memory segment containing at least one work queue, the work queue being in the form of a first-in-first-out instruction queue for the at least one functional unit.

18. (Previously presented) The system of claim 17, wherein the coherency mechanism further includes logic for responding to messages stored within the work queue to control read and write access to the RAM connected to the node.

19. (Currently Amended) A system, comprising:

a plurality of nodes and a random access memory (RAM) connected to each node; each node comprising:

a communication mechanism configured to manage and control communication of information with other nodes, the information being communicated within messages that are communicated among the nodes;

logic configured to manage a work queue within the connected RAM, wherein the work queue is populated by messages received from the plurality of nodes;

a memory controller configured to control writes to and reads from the RAM connected to the node, the memory controller being responsive to messages contained within the work queue; and

wherein the plurality of RAMs are collectively managed as a unified memory space such that data stored in one RAM is not duplicatively stored in another RAM, and wherein the memory controller of each node is configured to permit read access to the connected RAM both a functional unit within the connected node and by remote nodes, but the memory ~~mrmory~~ controller of each node is further configured to limit write access to the connected RAM to only the node to which the RAM is connected.

20. (Previously presented) A graphics processing system, comprising:

four nodes, wherein each node comprises a random access memory (RAM) coupled to a functional unit and a processor, the processor being coupled to the functional unit to direct data into and out of the functional unit, wherein each functional unit comprises a geometry accelerator coupled to a rasterizer and a memory controller; and

each of the four nodes being connected to each of the other three nodes through a communication link, and each of the four nodes adapted to send data from its RAM to each of the other three nodes through the communication link.

21. (Previously presented) The graphics processing system of claim 20 wherein each functional unit can communicate with each of the other three functional units to effect a sequence of actions in the other functional units.

22. (Previously presented) The graphics processing system of claim 21 wherein the sequence of actions comprises retrieving data from a first RAM of a first node and sending the data to a second RAM of a second node.

23. (Previously presented) In a computer graphics system implemented in a distributed, nodal architecture, a method for performing geometry accelerator computations comprising:

writing input/output (I/O) messages from a device driver on a host in the form of command/data buffers;

translating the command/data buffers into work queue messages;

writing the work queue messages to a host interface communication mechanism;

distributing the messages to a plurality of geometry accelerator work queues;

propagating to an output of each geometry accelerator all messages that are not directly executable by the geometry accelerators; and

producing, by each geometry accelerator, a work queue for shaders, wherein the work queue for shaders comprise messages denoting drawing primitives.